

Appl No. 10/016800**PATENT**
IBM Docket No. RAL920000126US1**Amendments to the Claims:**

1. (Currently Amended) A system comprising:
- a first ASIC (Application Specific Integrated Circuit) including a first substrate;
 - a plurality of On Chip Macros mounted on said first substrate;
 - a second ASIC including a second substrate positioned in spaced relationship to said first substrate;
 - a plurality of On Chip Macros mounted on said second substrate;
 - a Chip to Chip Non-Serial Bus Interface subsystem operatively positioned to provide communications between the first ASIC and the second ASIC; and
 - at least one on-chip non-serial ASIC bus coupled to at least one of the on-chip macros on the first and the second ASIC, respectively, wherein number of ~~bits~~ bit lines in the on-chip non-serial bus is greater than the number of ~~bits~~ bit lines in the non-serial Bus Interface subsystem; and
 - a Chip to Chip Macro subsystem operatively mounted on the first ASIC and the second ASIC, said Chip to Chip Macro subsystem receiving data with a first footprint equivalent to number of ~~bits~~ bit lines in the on-chip non-serial ~~non-serial~~ ASIC bus reducing the first footprint so the data matches footprint of the chip to chip non-serial bus interface subsystem ~~aggregating all communications between at least a pair of On Chip Macros one of each being located on the first substrate and the second substrate onto the Chip to Chip Bus Interface subsystem.~~
2. (Original) The system of Claim 1 wherein the Chip to Chip bus interface subsystem includes a first transmission system transmitting data from the first ASIC to the second ASIC; and
- a second transmission system transmitting data from the second ASIC to the first ASIC.

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- 1 3. (Original) The system of Claim 2 wherein the first transmission system includes a
2 first unidirectional data bus;
3 a first unidirectional parity bus;
4 a first unidirectional start of message control line; and
5 a first unidirectional clock bus.
- 1 4. (Original) The system of Claim 3 wherein the first transmission system further
2 includes a first control line that transmits a signal in a direction opposite to signal
3 transmisslon on other lines in said first transmission system, said signal inhibiting a
4 Macro on a selected ASIC from transmitting data.
- 1 5. (Currently Amended) The system of Claim ~~[[2]]~~ 3 wherein the second transmission
2 system includes a set of transmission lines substantially similar to those set forth in
3 Claim ~~[[4]]~~ 3.
- 1 6. (Currently Amended) The system of Claim 5 further Including a second control line
2 that transmits signals in a direction opposite to signal transmission on other the set
3 of transmission lines in said second transmission system ~~systems~~.
- 1 7. (Original) The system of Claim 1 wherein the Chip to Chip Macro subsystem
2 includes a first Chip to Chip Macro operatively mounted on the first ASIC; and
3 a second Chip to Chip macro operatively mounted on the second ASIC.

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1 8. (Original) The system of Claim 7 wherein the first Chip to Chip macro or the
2 second Chip to Chip macro includes a transmit (Tx) channel; and
3 a Receive Channel wherein said Tx channel includes a transmitter Multiplexor;
4 a transmitter Speed Matching Buffer connected in series to the transmitter
5 Multiplexor; and
6 a Serializer connected in series to the transmitter speed matching buffer; and said
7 Receive Channel includes a De-serializer; Receive (Rx) Speed Matching buffer connected
8 in series to the De-Serializer and a Rx De-multiplexor connected in series to the Rx Speed
9 Matching buffer.

1 9. (Currently Amended) The system of Claim 8 wherein the Tx Multiplexor further
2 includes arbitration devices receiving requests from multiple Macros and granting
3 priority to transmit to one of said ~~requests~~ multiple macros; and
4 a generator, response to ~~the a request from~~ one of said multiple macros, ~~requests~~
5 to generate a message based upon information in ~~the one of said requests~~ request from
6 one of said multiple macros and forward said message to the speed matching buffer.

1 10. (Original) The system of Claim 8 wherein the Rx De-multiplexor includes a
2 decoder that decodes selected fields in messages to determine which Macro
3 should receive the message.

1 11. (Currently Amended) A Macro for interconnecting chips comprising:
2 a Transmit channel; and
3 a Receive channel; said Transmit Channel including an arbitrator that arbitrates
4 Requests generated from multiple Requesters and granting priority to one of the requests;
5 a generator responsive to said one of the requests to generate a first message
6 based upon information in said one of the requests;

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7 a first Speed Matching Buffer that receives the first message; and
8 a Serializer extracting the first message ~~messages~~ from said Speed Matching
9 Buffer at a first data rate over a ~~relatively wide~~ first parallel data bus and converting said
10 message to a second data rate for transmission over a second parallel data bus wherein
11 ratio of bit lines in the first parallel data bus and the second parallel data bus are different
12 ~~narrower than the relatively wide data bus.~~

1 12. (Original) The Macro of Claim 11 wherein the Speed Matching Buffer includes a
2 RAM; and
3 a controller coupled to said RAM, said controller causing data to be written in said
4 RAM at a first frequency and read from said RAM at a different frequency.

1 13. (Currently Amended) The Macro of Claim 11 wherein the Receive Channel further
2 includes
3 a second Speed Matching Buffer that buffers messages received from another
4 macro;
5 a De-serializer receiving the messages having a first footprint and the second first
6 data rate from another macro, said De-serializer adjusting the first second footprint and
7 first the second data rate of the messages from another macro and loading said
8 ~~messages~~ message into the second Speed Matching Buffer; and
9 a De-Multiplexor including circuits to extract said ~~messages~~ message from the
10 Speed Matching Buffer, determining destination of said ~~extracted messages~~ message
11 and forwarding the extracted message to determined destinations.

1 14. (Original) The Macro of Claim 12 further including circuit in said second Speed
2 Matching Buffer to generate a control signal if said second speed matching buffer
3 does not wish to receive additional data.

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- 1 15. (Original) The Macro of Claim 11 or Claim 13 further including
2 a Network Processor Complex Chip operatively coupled to said Macro.
- 1 16. (Original) The Macro of Claim 11 or Claim 13 further including
2 a Scheduler Chip operatively coupled to said Macro.
- 1 17. (Original) The Macro of Claim 11 or Claim 13 further including a Data Flow Chip
2 operatively coupled to the Macro.
- 1 18. (Currently Amended) A method comprising:
2 partitioning circuits into functional blocks on a first ASIC and a second ASIC;
3 generating Request signals by functional blocks on the first ASIC wanting to
4 communicate with functional blocks on the second ASIC;
5 granting priority to one Request based upon a result of an arbitrator arbitrating
6 between multiple Requests;
7 generating a message based upon information in the one Request;
8 buffering the message in a first buffer; and
9 serializing buffered messages with a Serializer to permit data transmitted at a first
10 data rate on a parallel wide internal ASIC bus to be transferred on a narrower another
11 parallel bus at a higher data rate wherein the parallel internal ASIC bus includes more bit
12 data line than the another parallel bus.
- 1 19. (Currently Amended) The method of Claim 18 wherein the parallel internal ASIC
2 bus is approximately 128 bits.

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- 1 20. (Currently Amended) The method of Claim 19 wherein the ~~narrower~~ another
2 parallel bus is approximately 32 bits and the higher data rate is approximately
3 500Mbit/sec (per bit).
- 1 21. (Currently Amended) The method of Claim 18 further including ~~the steps of~~
2 providing on the first ASIC a second buffer to receive messages from the second
3 ASIC;
4 converting the message by a De-serializer from a first footprint, equivalent to a
5 width of a first bus, and first data rate to a second footprint, equivalent to a width of a
6 second bus, and second data rate; and
7 writing converted messages into the second buffer.
- 1 22. (Currently Amended) The method of Claim 21 further including ~~the steps of~~
2 extracting by a De-multiplexor messages from said second buffer;
3 determining by said De-multiplexor a destination for said extracted messages; and
4 forwarding said extracted messages to the destination.
- 1 23. (Original) The system of Claim 1 wherein the first ASIC includes a Network
2 Processor Complex Chip and the second ASIC includes a Data Flow Chip.
- 1 24. (Original) The system of Claim 1 where the first ASIC includes a Data Flow Chip
2 and the second ASIC includes a Scheduler chip.
- 1 25. (Currently Amended) A system comprising:
2 a Data Flow Chip;
3 a first Chip to Chip Macro operatively mounted on said Data Flow Chip;
4 a Scheduler Chip;

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5 a second Chip to Chip Macro operatively mounted on said ~~Data Flow~~ Schedule
6 Chip;
7 a transmission interface interconnecting the first Chip to Chip Macro and second
8 Chip to Chip Macro.

1 26. (Currently Amended) A device comprising:
2 an ASIC having circuits that can be grouped into separate sub Macros; and
3 a Chip to Chip Macro mounted on said ASIC, said Chip to Chip macro receiving
4 data at a first data rate with a first footprint from selected ones of said sub Macros
5 converting the data to a second footprint at a second data rate and transmitting the data at
6 the second data rate and second footprint wherein said first footprint mirrors that of a first
7 parallel bus having n bit data lines and said second footprint mirrors that of a second
8 parallel bus having m bit data lines, with n greater (>) than m and n and m being numbers >
9 1.

1 27. (Currently Amended) The device of Claim 26 wherein the second footprint is
2 narrower includes fewer data lines than the first footprint and the second data rate is
3 higher than the first data rate.